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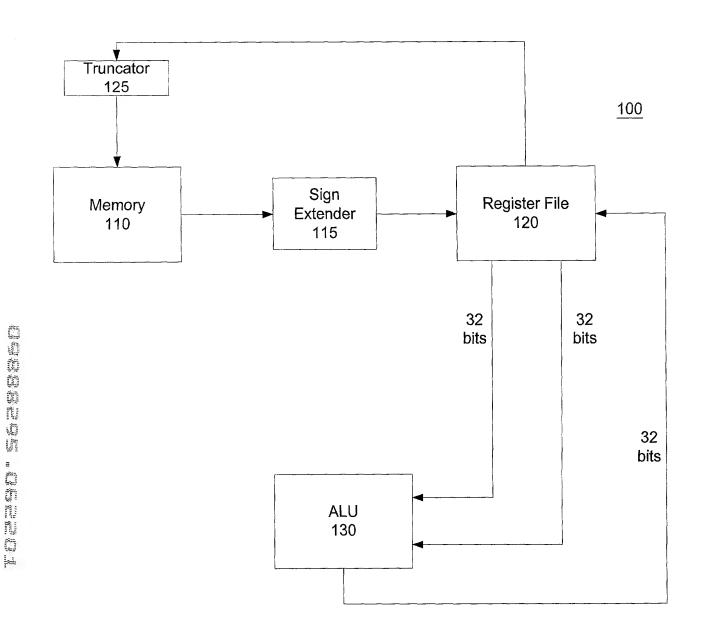


Figure 1A

SET; Inventors: David A. Fotiand et al.;

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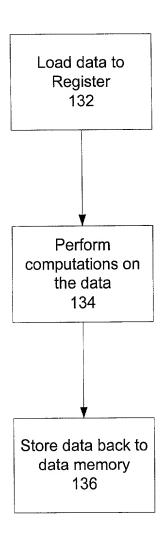


Figure 1B

SET; Inventors: David A. Fotland et al.;

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OPCode 6 bits	Source1 Register 5 bits	Source2 Register 5 bits	Target Register 5 bits	Sub-OPCode 11 bits
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Figure 1C

OPCode 6 bits	Target Register 5 bits	Source1 Register 5 bits	Immediate 16 bits
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Figure 1D



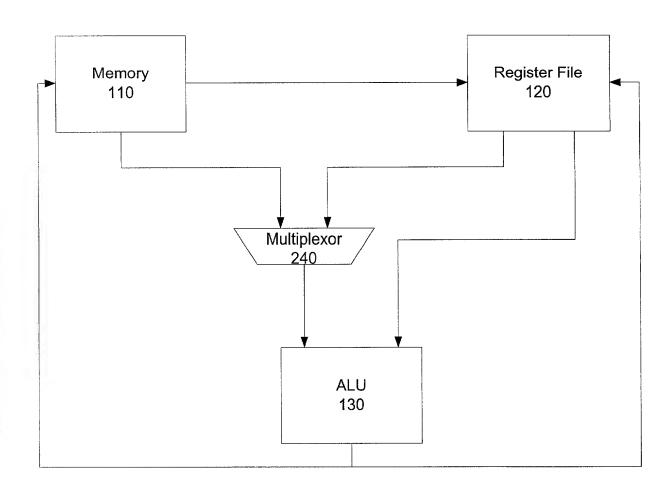


Figure 2

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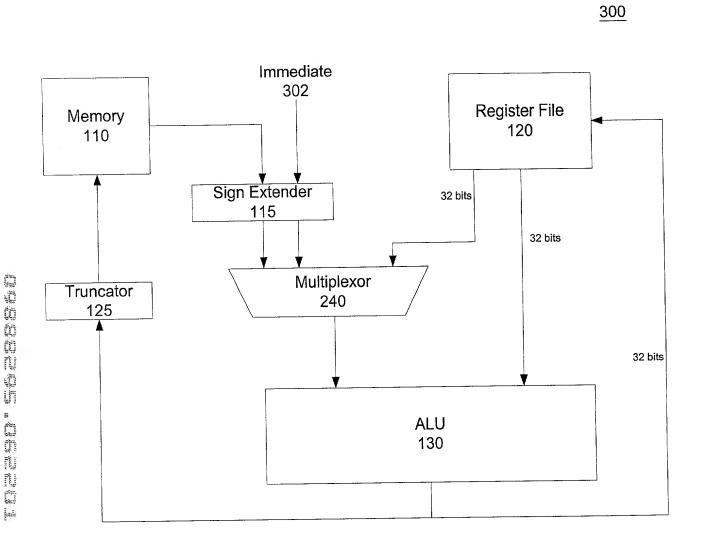
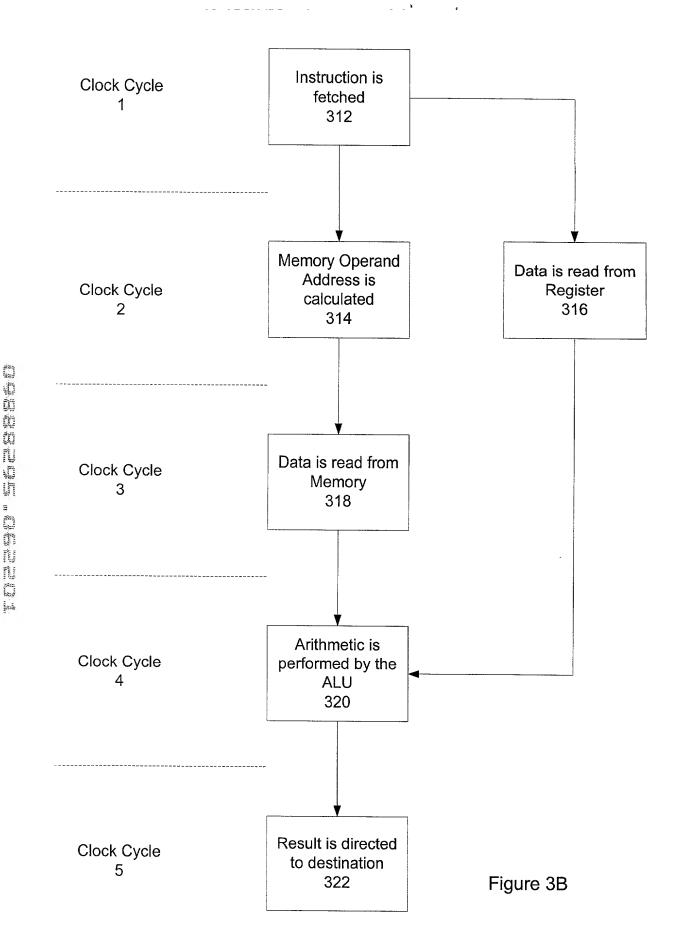


Figure 3A



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<u>400</u>

OPCode 5 bits	Destination 11 bits	Source2 Register 5 bits	Source1 11 bits
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Figure 4

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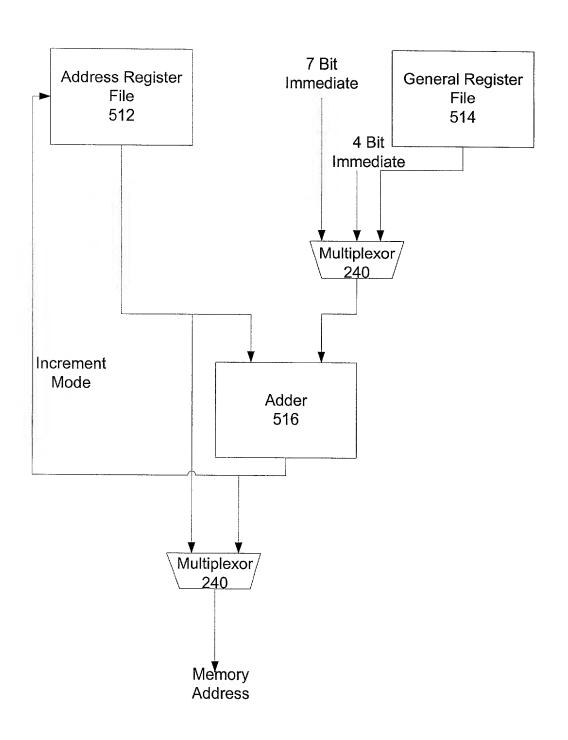


Figure 5

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1	I ₆	l ₅	14	l ₃ l ₂ l ₁ l ₀
0	1	1	$A_2A_1A_0$ R_4	$R_3 R_2 R_1 R_0$
0	1	0	M	l_3 l_2 l_1 l_0
0	0	1	Register Direct	
0	0	0	Immediate	

Row 1

Row 2

Row 3

Row 4

Row 5

Figure 6

SET; Inventors: David A. Fotland et al.;

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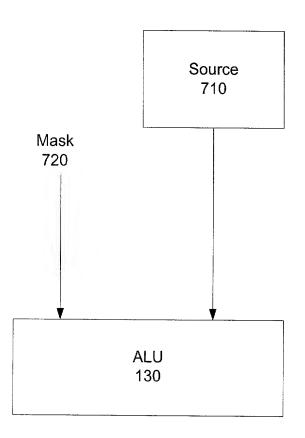


Figure 7

SET; Inventors: David A. Fotland et,al.;

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Word 2

Load

Shift & Merge

The state of the s

Figure 8

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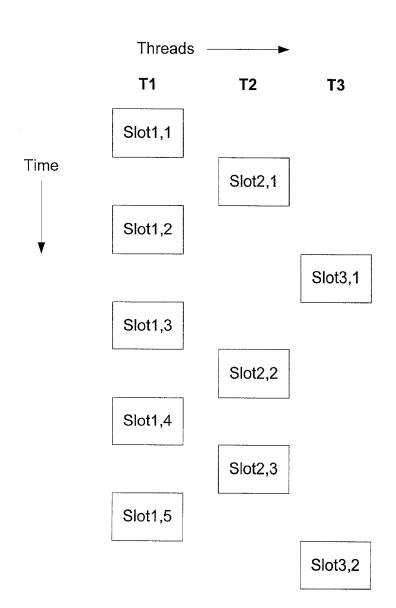


Figure 9